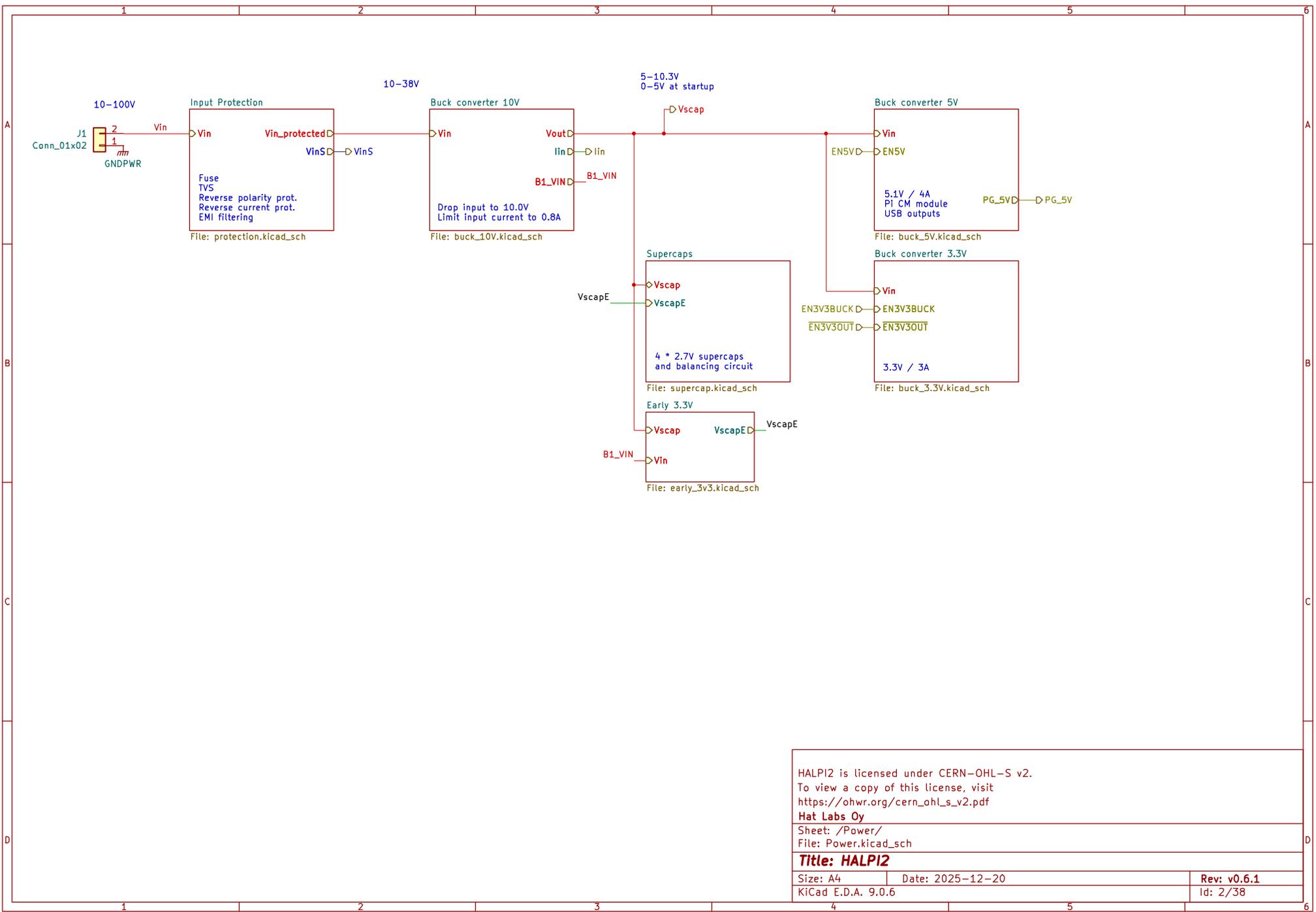


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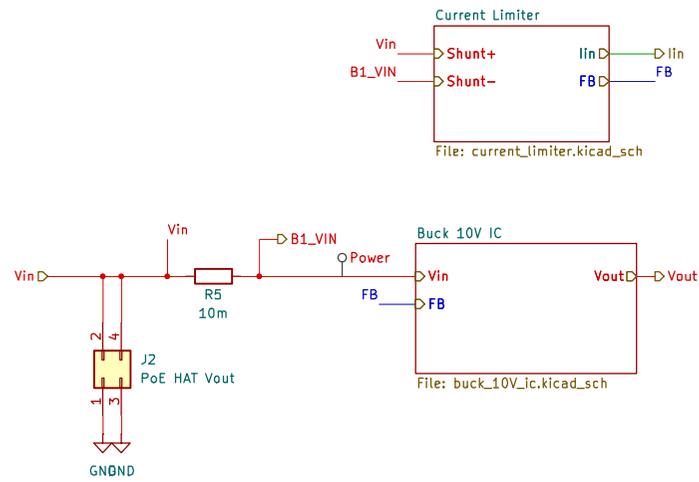
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KiCad E.D.A. 9.0.6	Rev: v0.6.1
	Id: 1/38



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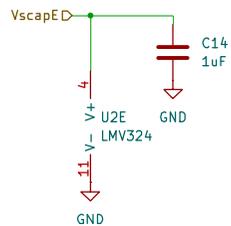
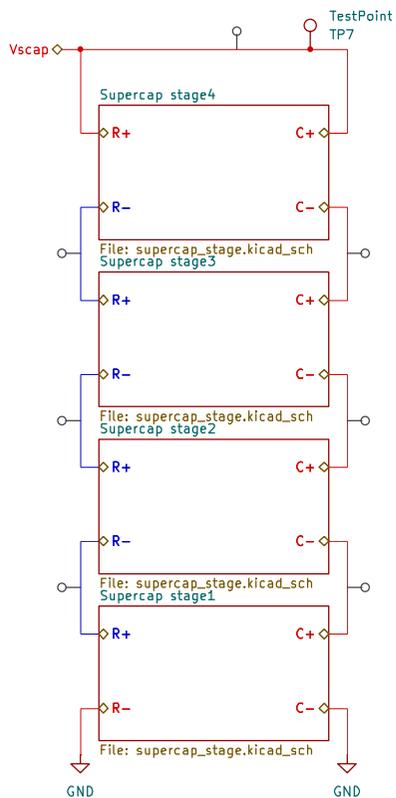
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Supercapacitor balancing circuit modeled after
<https://www.eevblog.com/forum/renewable-energy/supercapacitor-balancer/>



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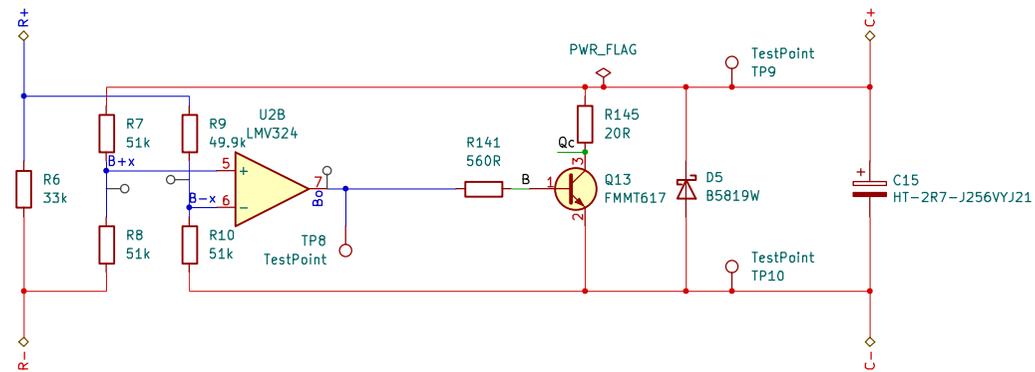
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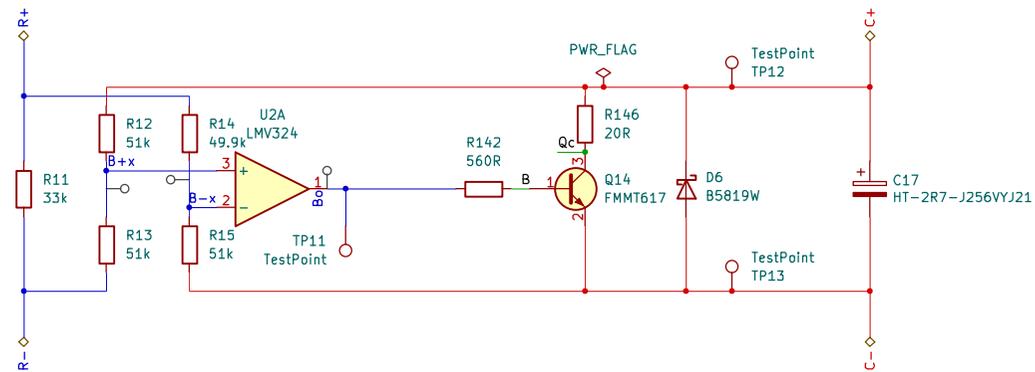
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Rev: v0.6.1
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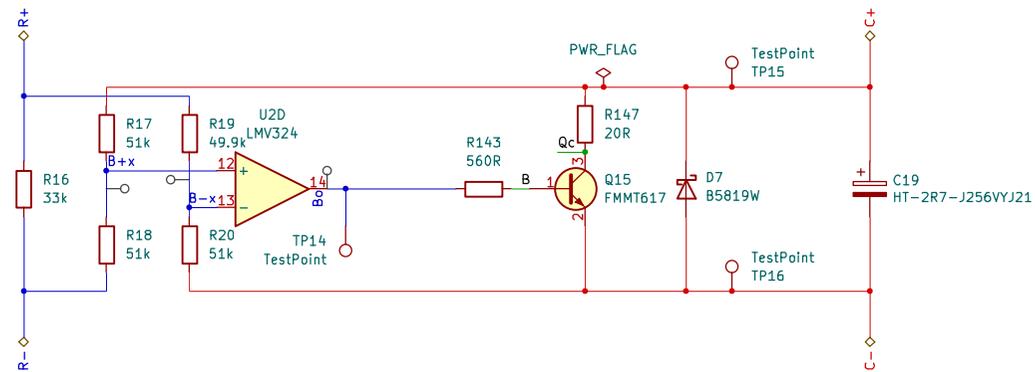
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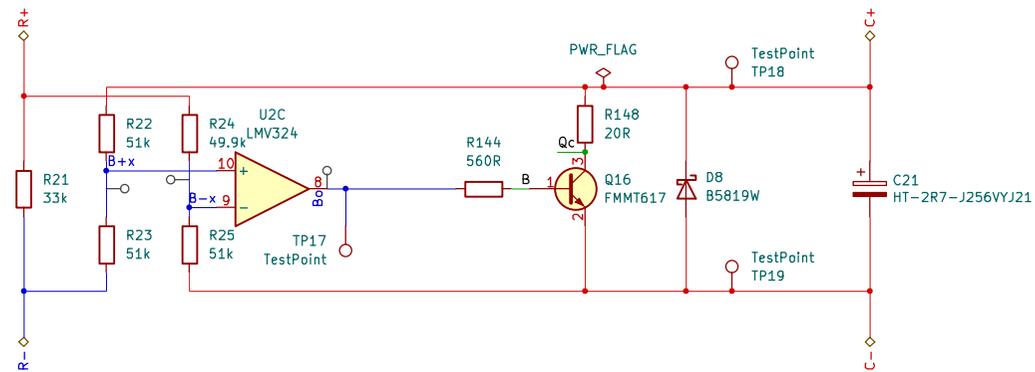
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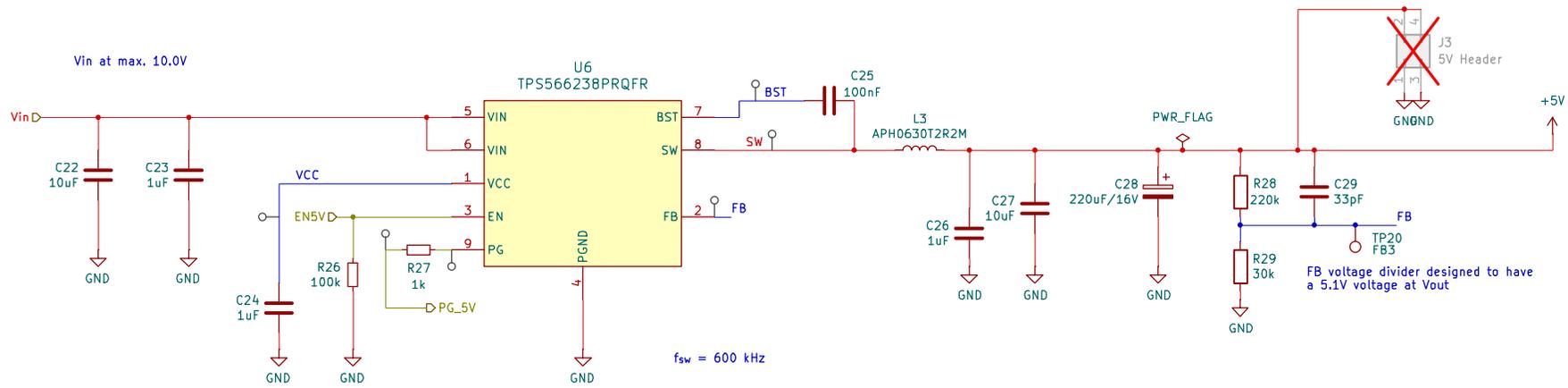
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Title: HALPI2

Size: A4 Date: 2025-12-20
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Buck converter dropping the supercap voltage down to 5V for the CM4/5 module input and USBs



FB voltage divider designed to have a 5.1V voltage at Vout

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Sheet: /Power/Buck converter 5V/
File: buck_5V.kicad_sch

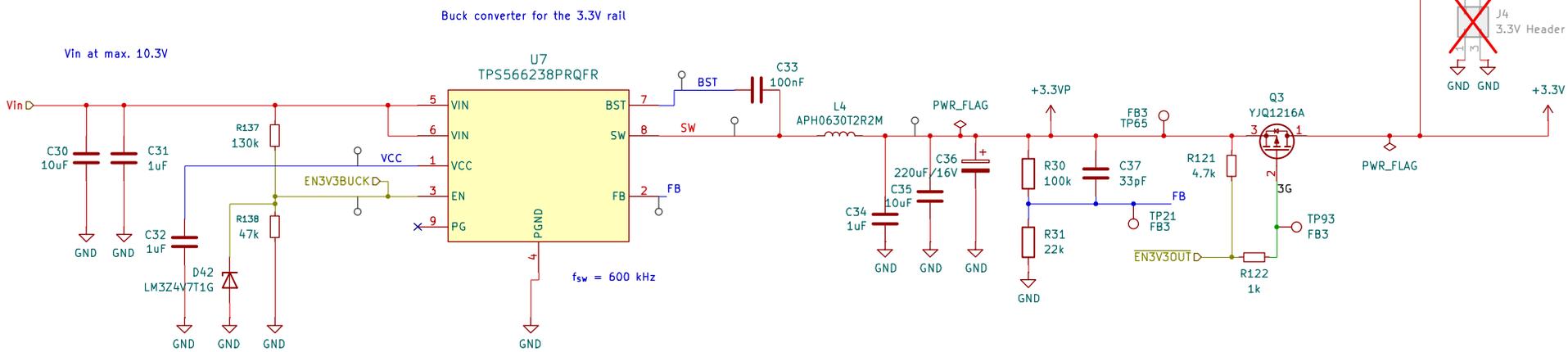
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Id: 10/38



Vin at max. 10.3V

Buck converter for the 3.3V rail

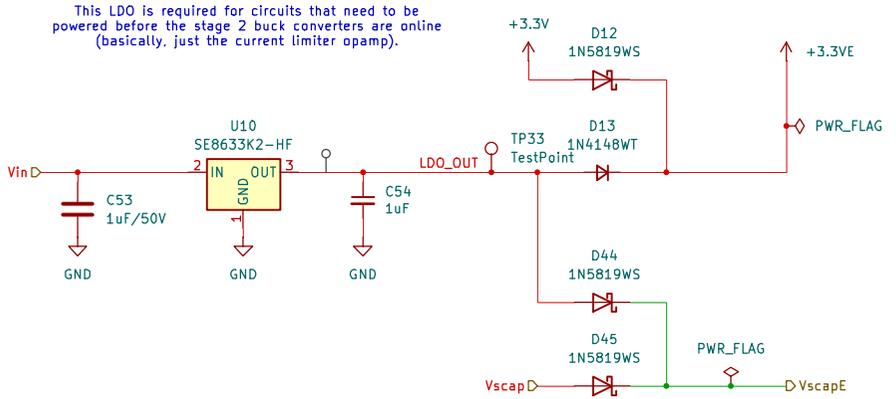
UVLO at 4.5V

fsw = 600 kHz

FB voltage divider designed to have a 3.33V voltage at Vout

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Size: A4	Date: 2025-12-20	Rev: v0.6.1
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This LDO is required for circuits that need to be powered before the stage 2 buck converters are online (basically, just the current limiter opamp).

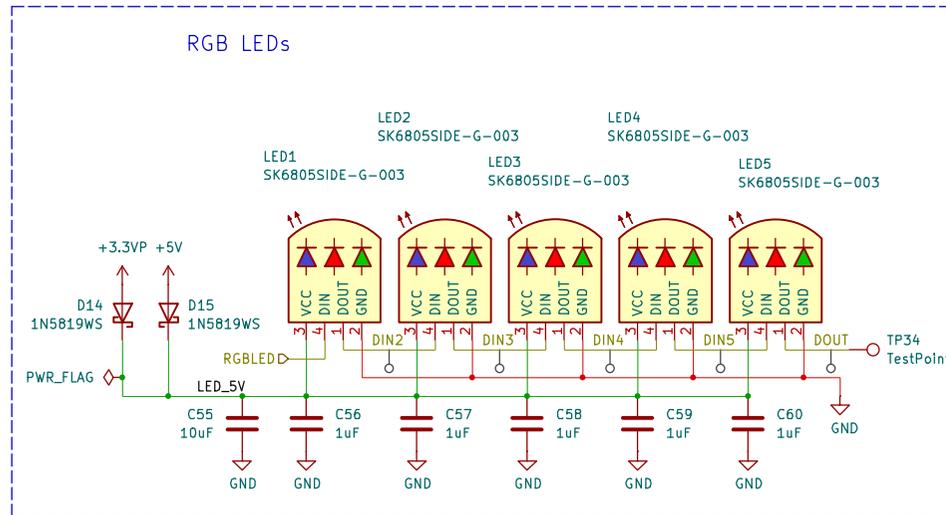
VscapE is used to ensure the supercap balancing circuit op-amps are powered immediately.

During undervoltage, TTL op-amps may be at a high state, causing all balancing NPNs to conduct before voltage is increased.

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File: early_3v3.kicad_sch

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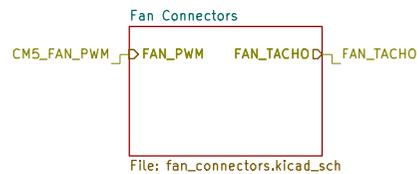
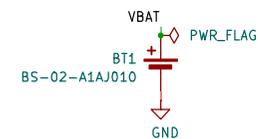
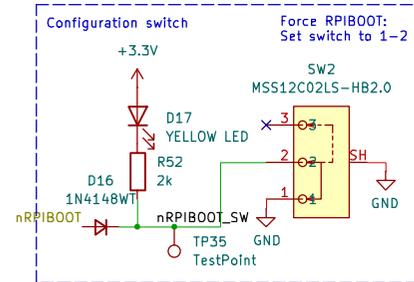
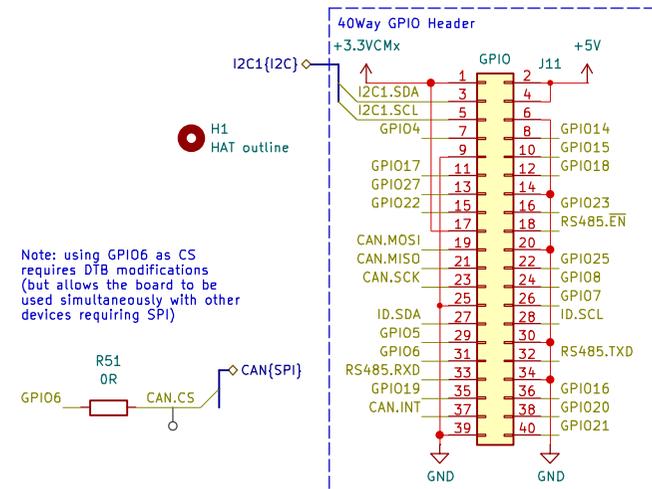
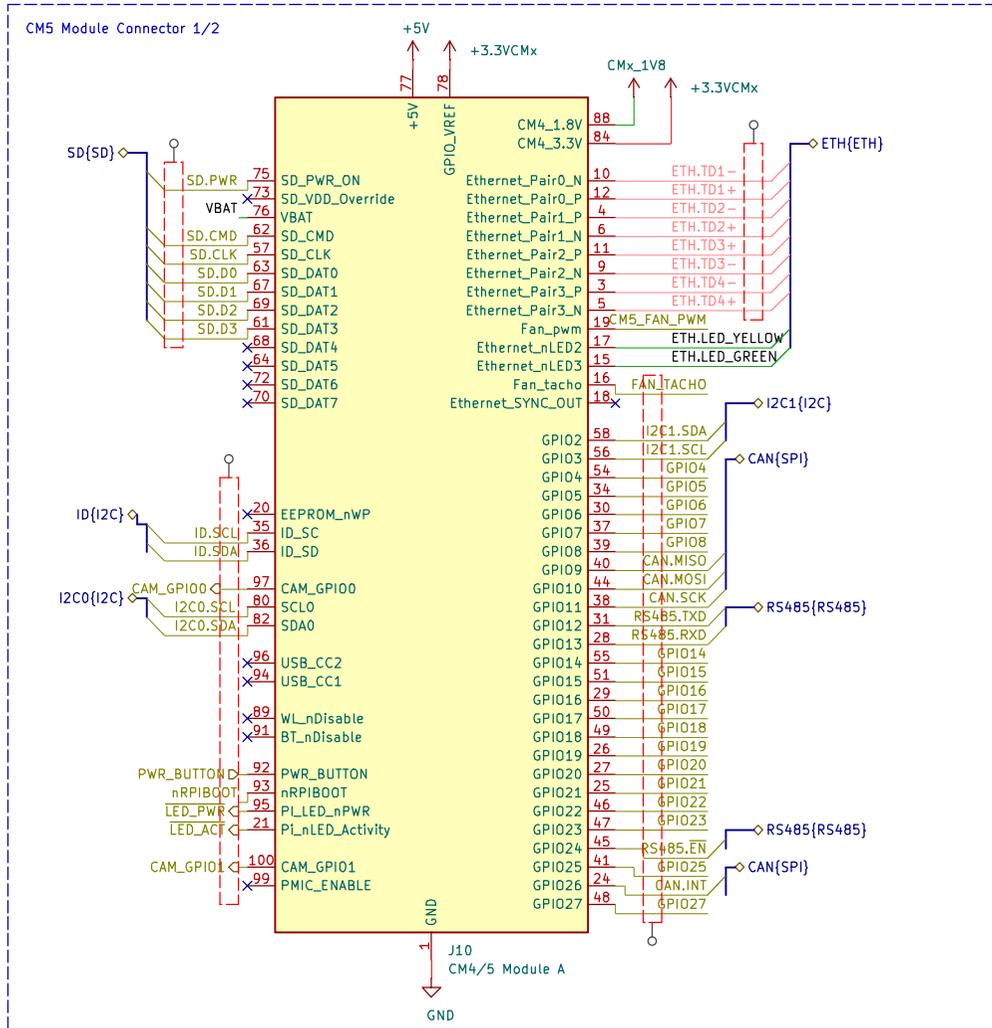
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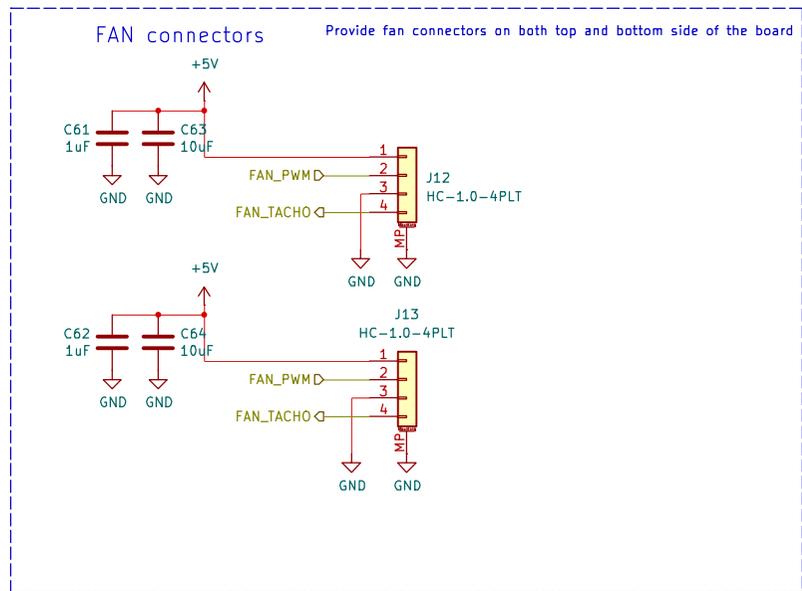
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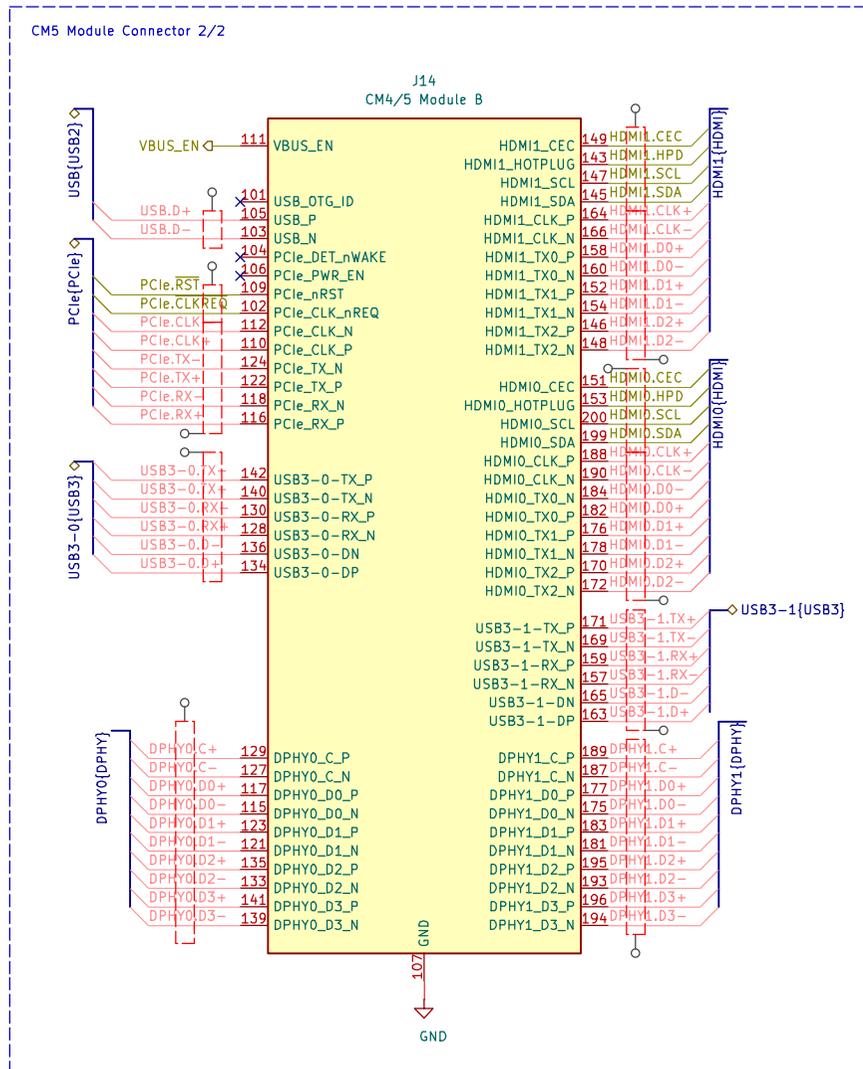
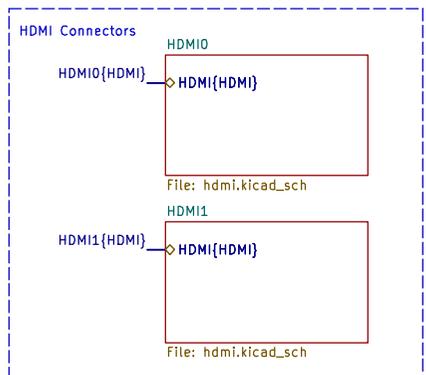
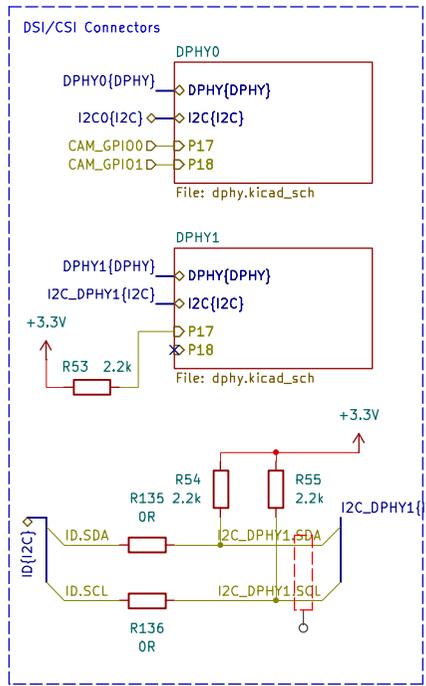
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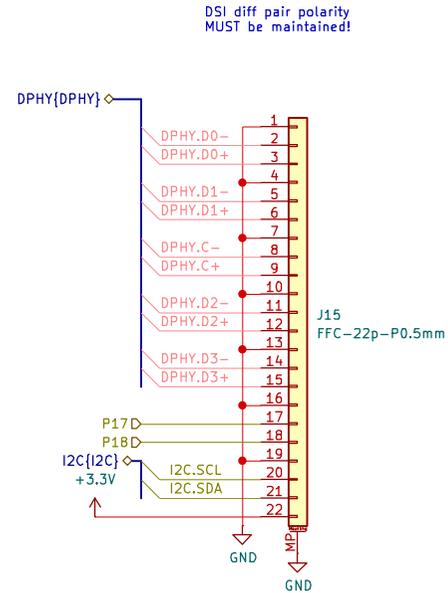
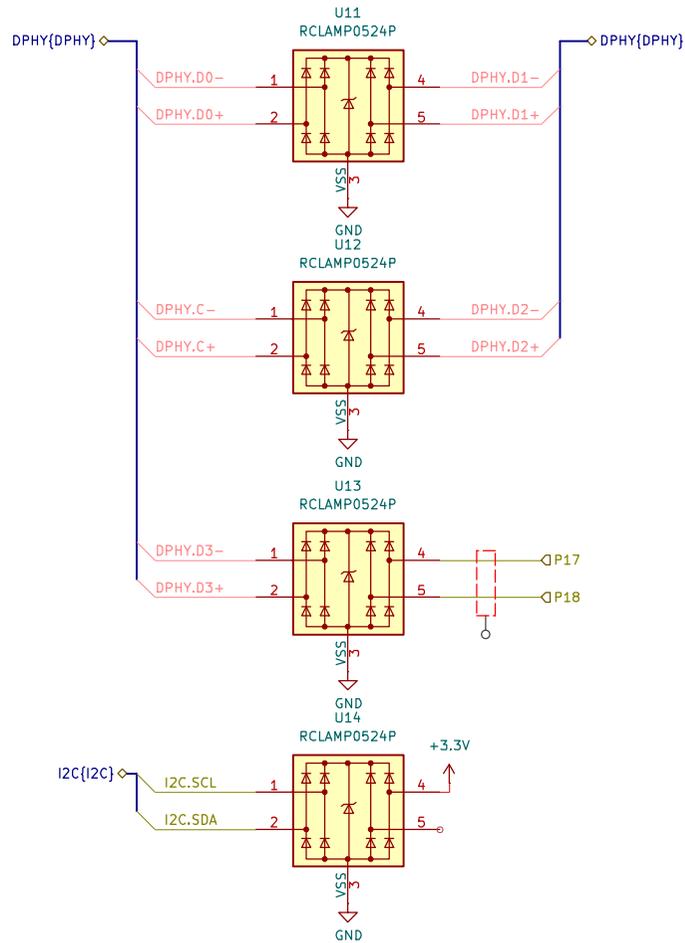
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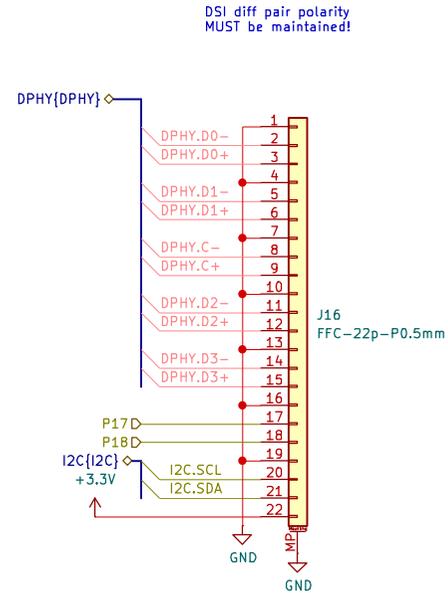
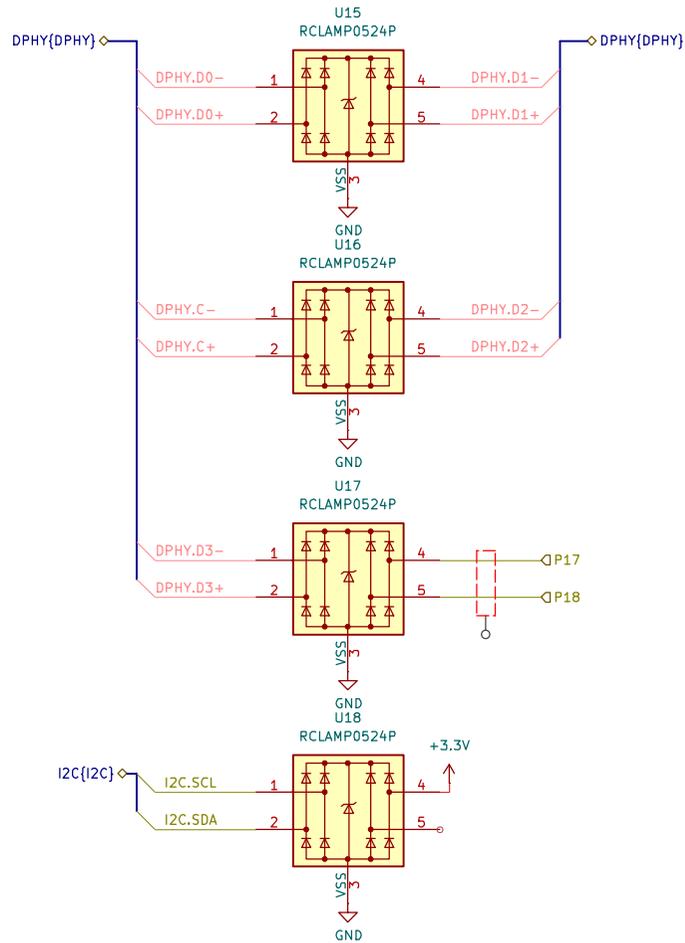
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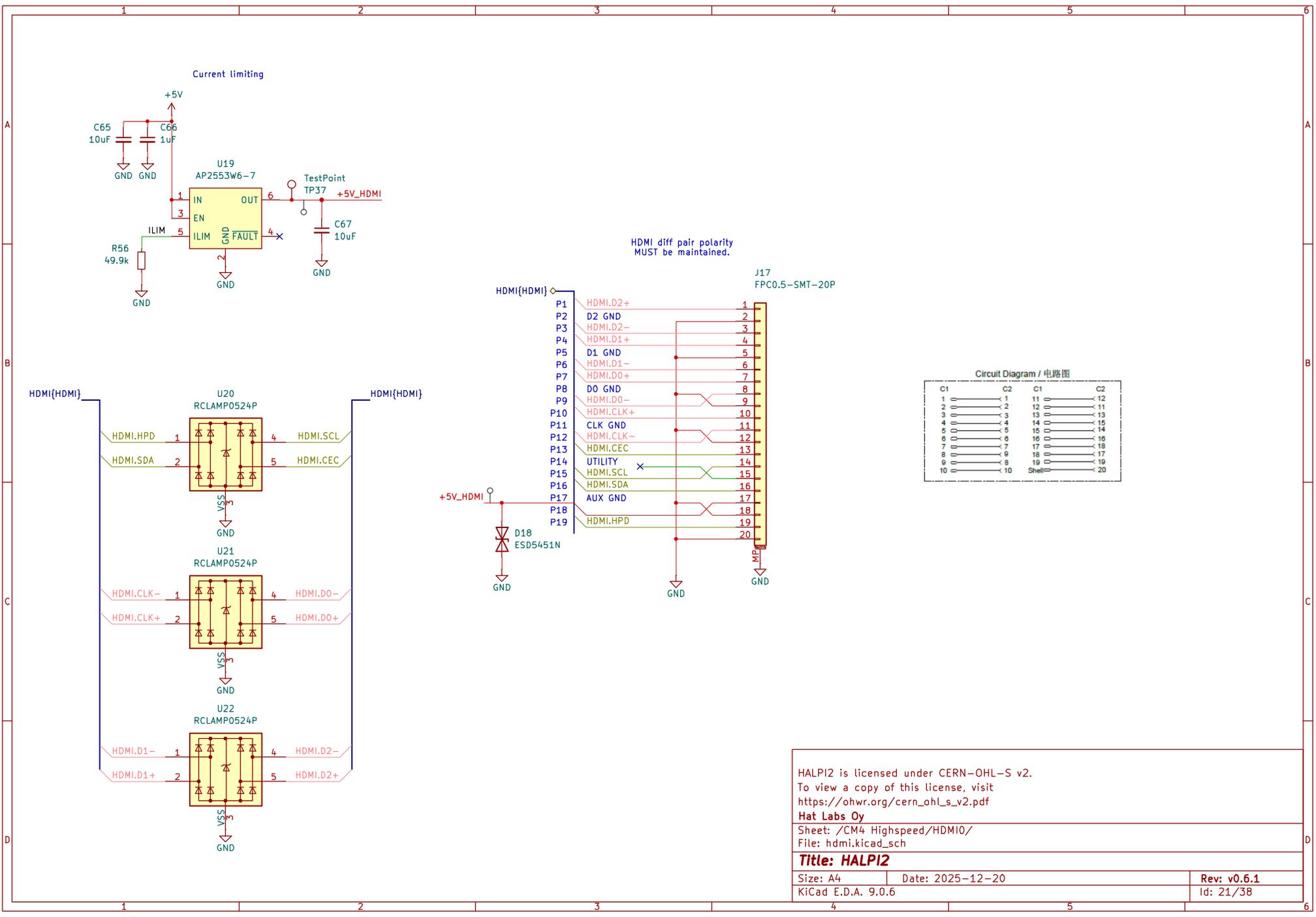
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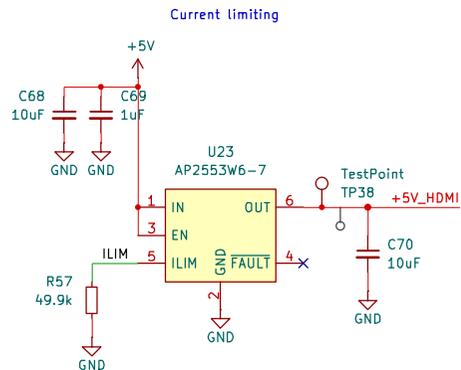
Circuit Diagram / 电路图

C1	C2	C1	C2
1	1	11	12
2	2	12	11
3	3	13	13
4	4	14	15
5	5	15	14
6	6	16	16
7	7	17	18
8	8	18	17
9	8	19	19
10	10	Shell	20

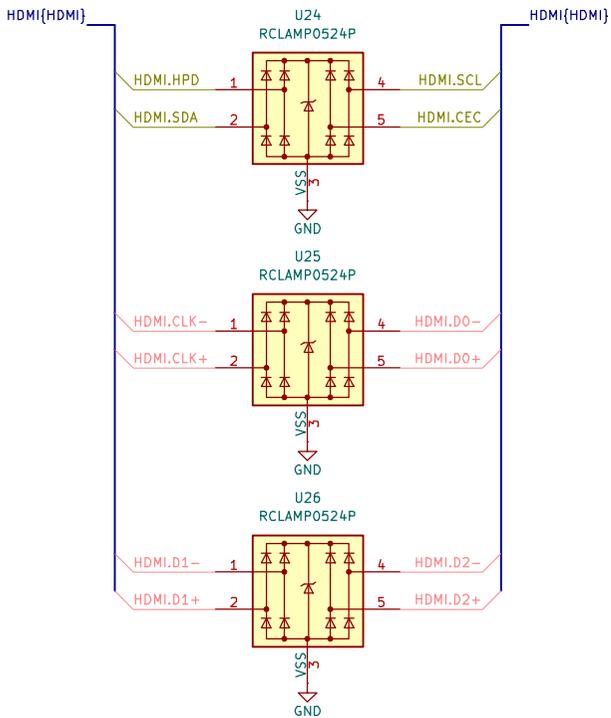
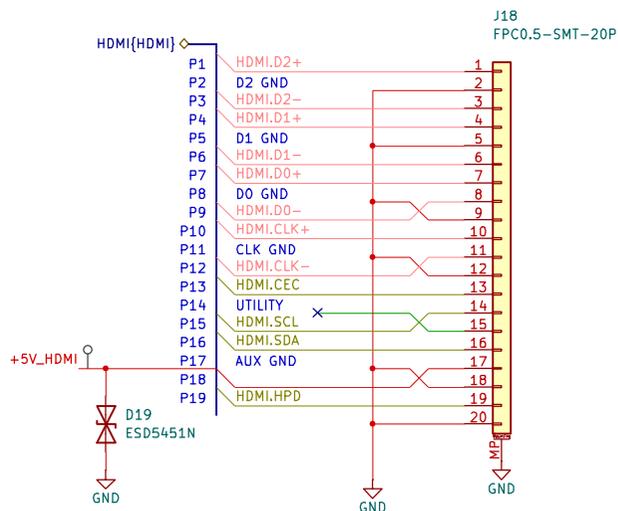
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HDMI diff pair polarity
MUST be maintained.



Circuit Diagram / 电路图

C1	C2	C1	C2
1	1	11	12
2	2	12	11
3	3	13	13
4	4	14	15
5	5	15	14
6	6	16	16
7	7	17	18
8	8	18	17
9	8	19	19
10	10	Shell	20

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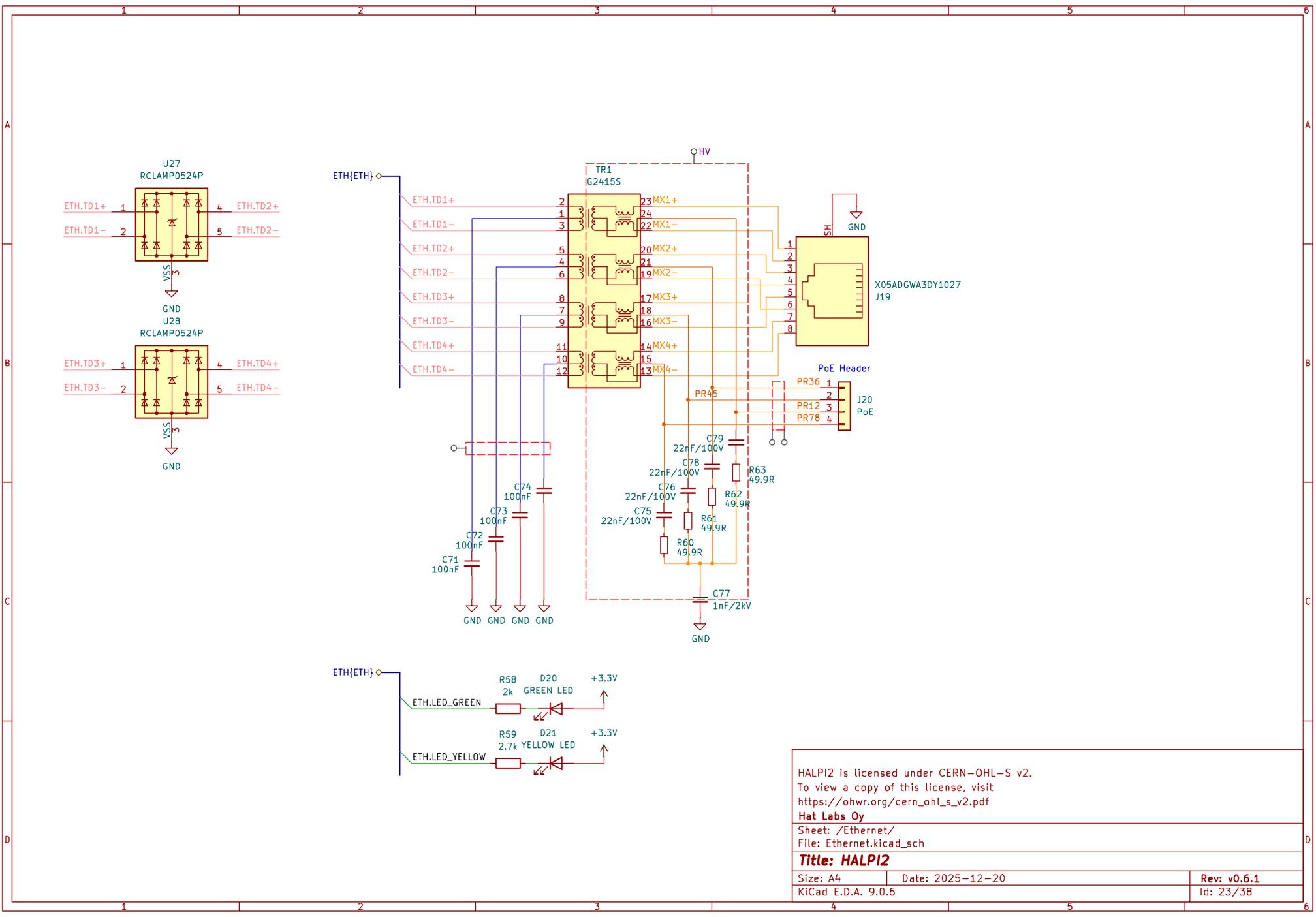
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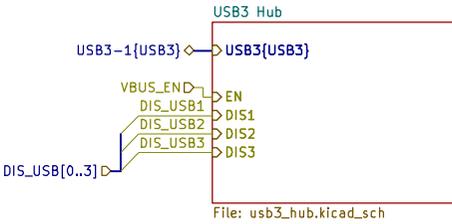
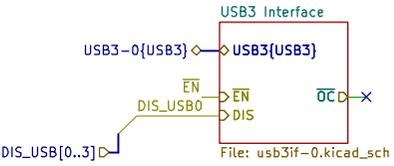
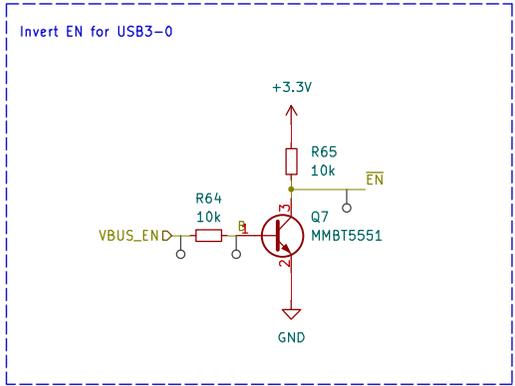
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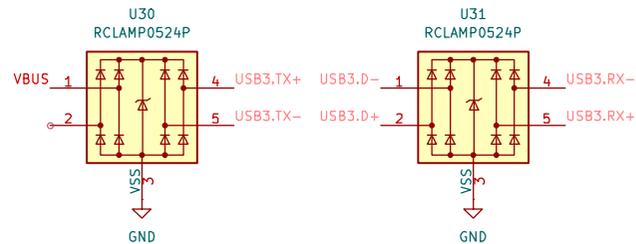
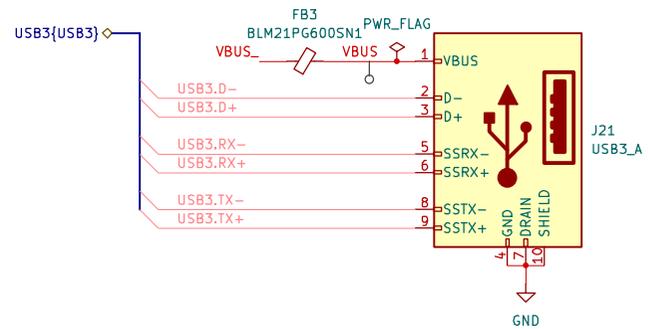
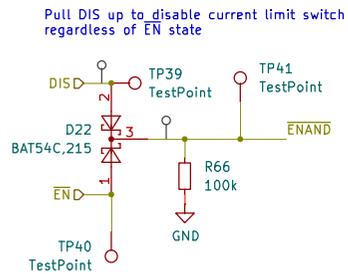
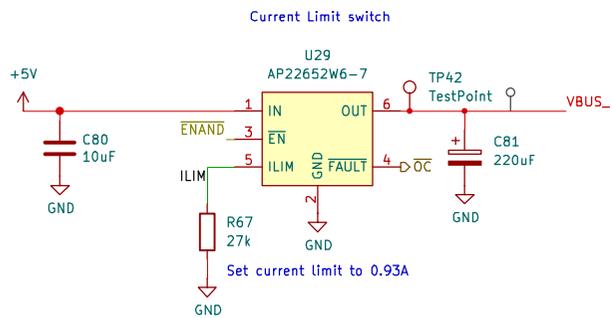
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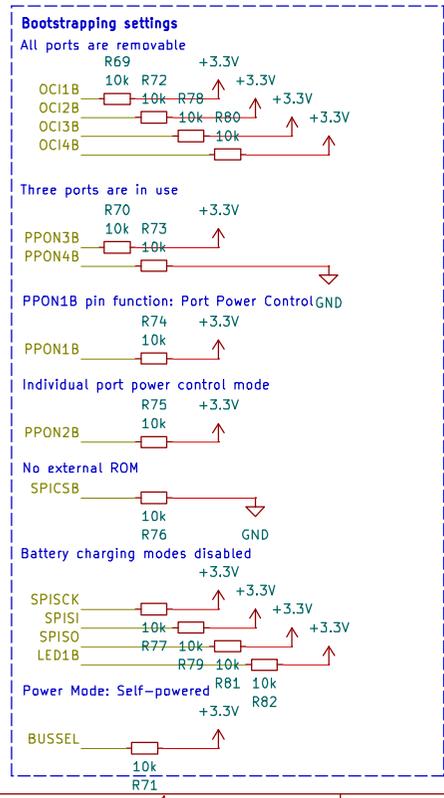
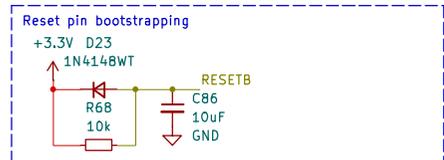
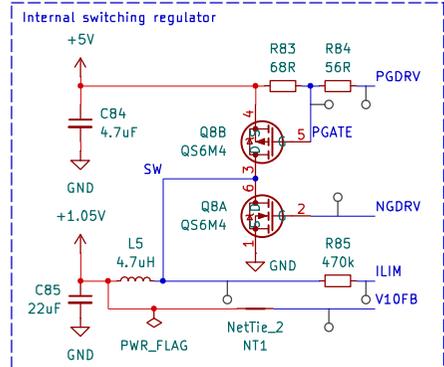
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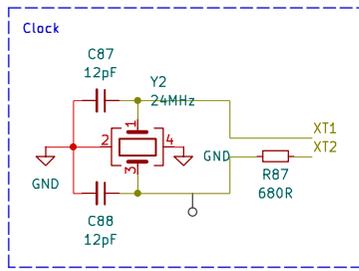
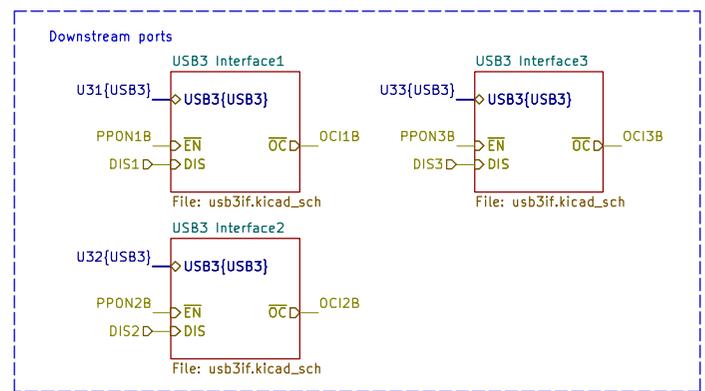
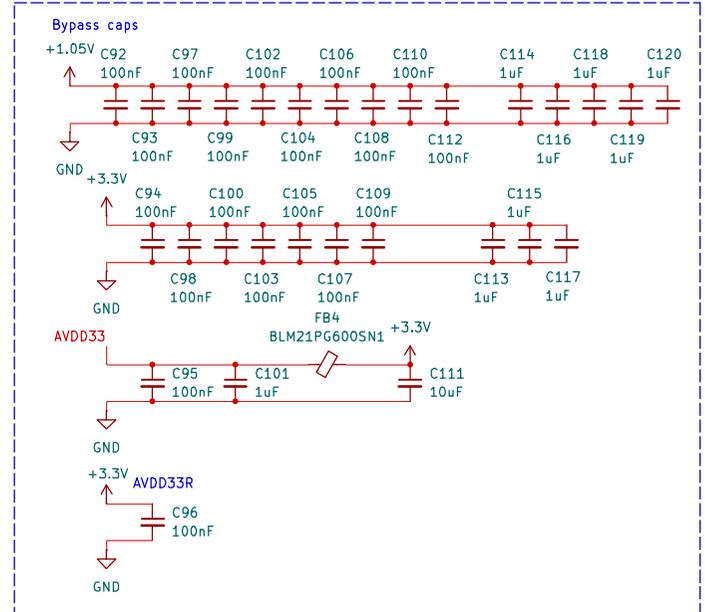
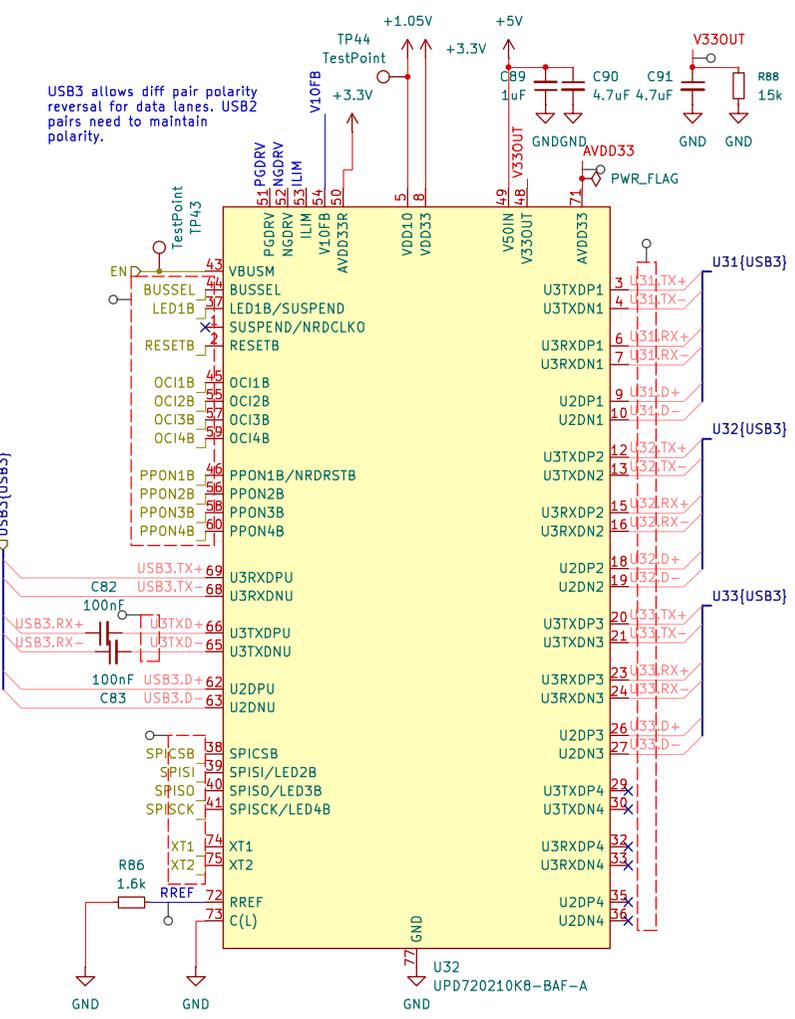
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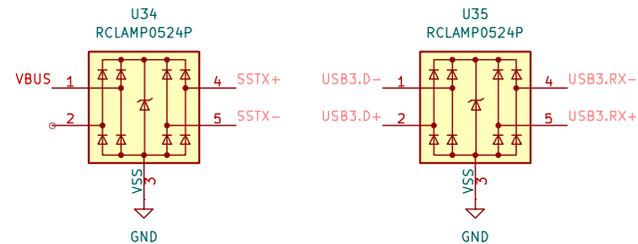
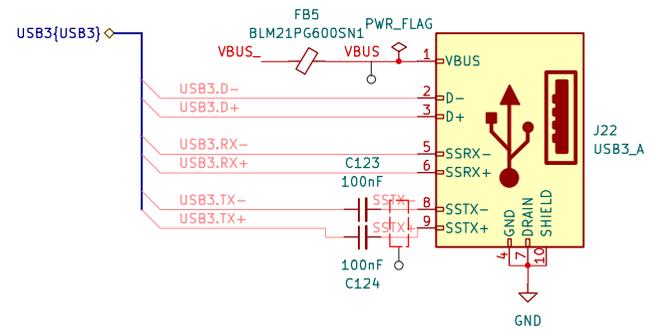
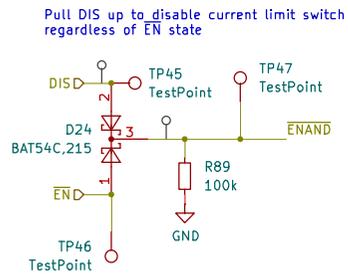
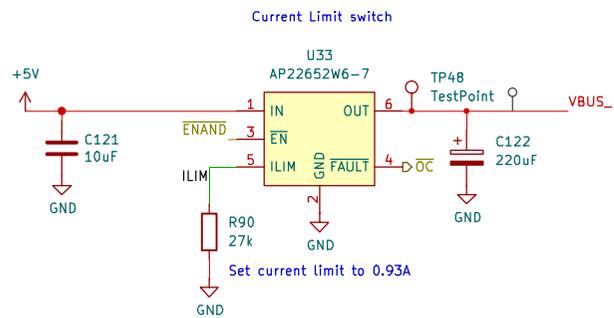
USB3 allows diff pair polarity reversal for data lanes. USB2 pairs need to maintain polarity.



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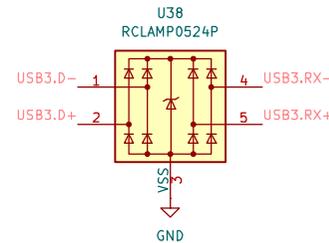
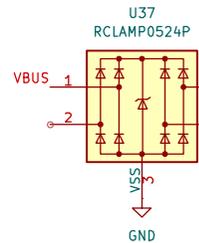
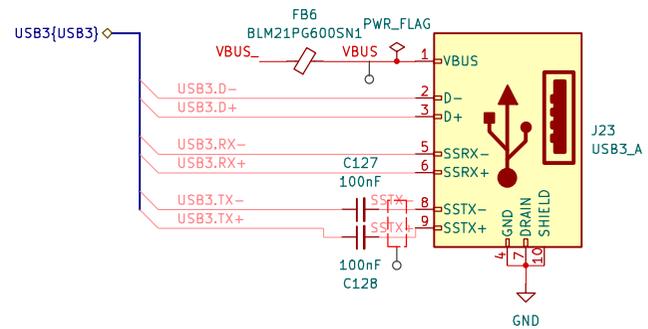
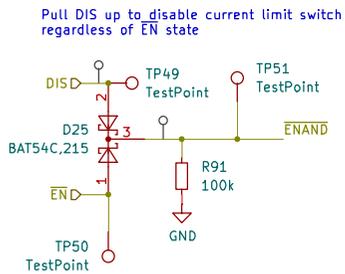
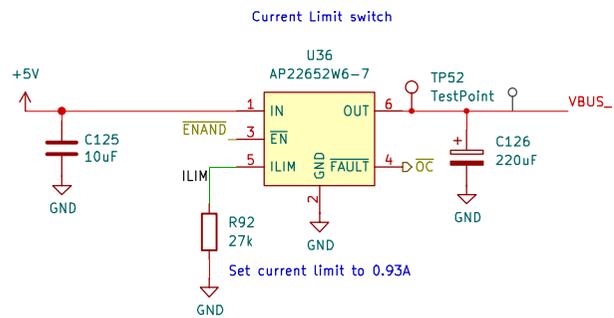
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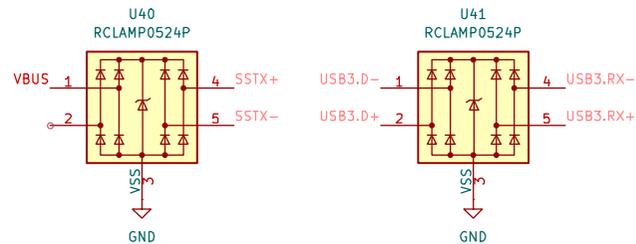
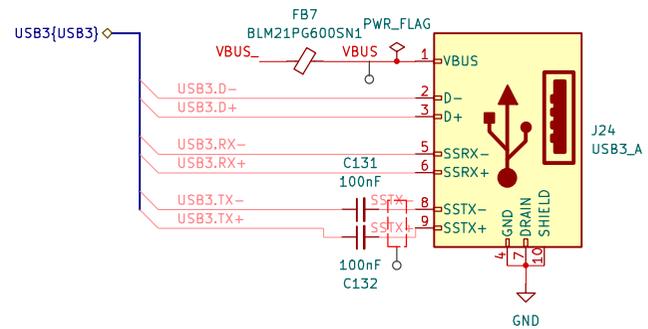
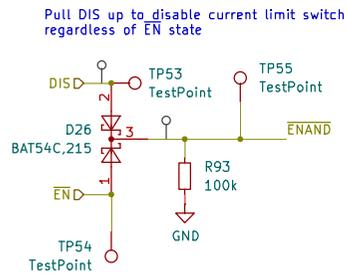
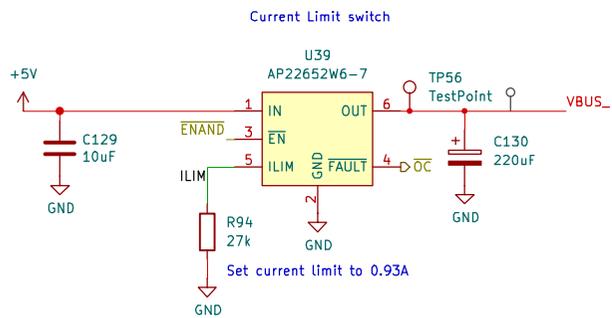
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Rev: v0.6.1

KiCad E.D.A. 9.0.6

Id: 28/38



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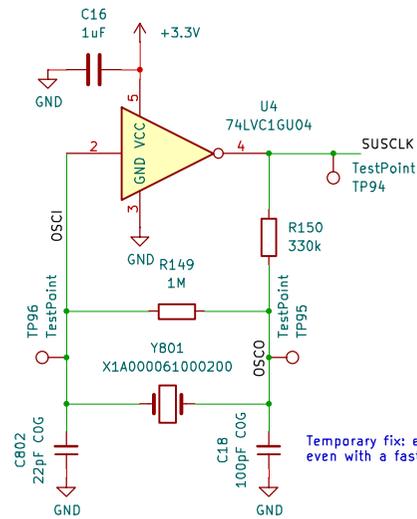
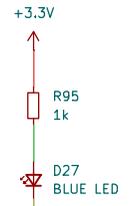
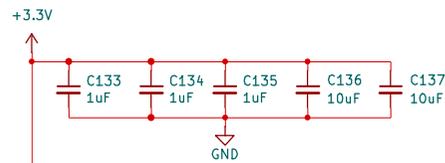
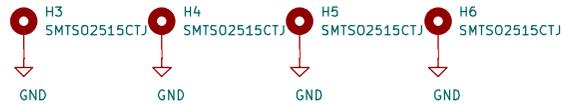
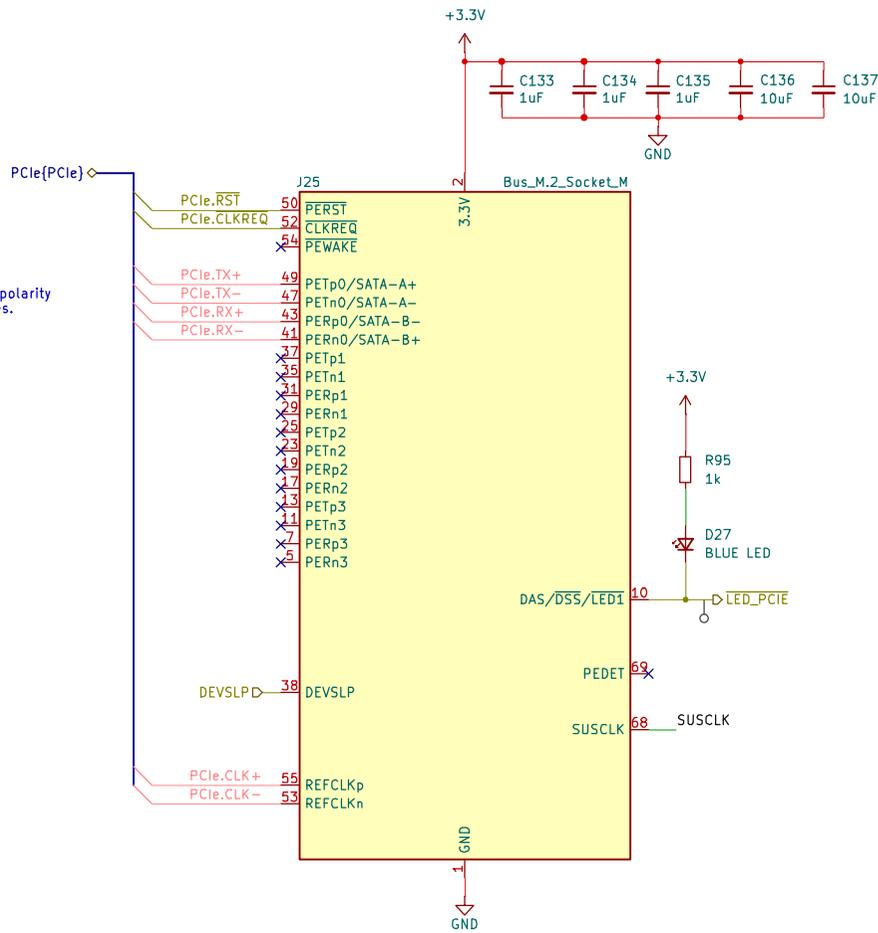
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Size: A4 Date: 2025-12-20
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PCIe allows diff pair polarity reversal for data lanes.



Temporary fix: ensure the oscillator starts even with a fast 74LVC inverter.

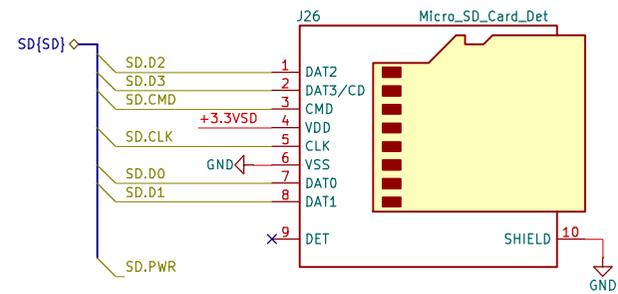
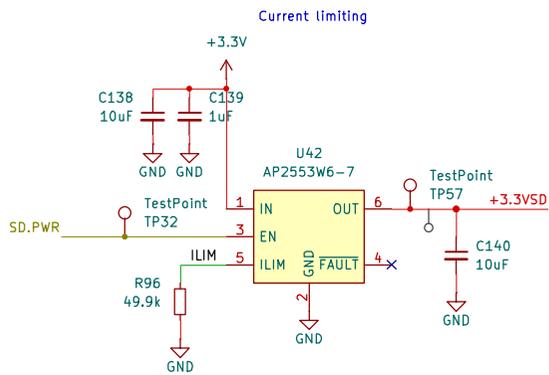
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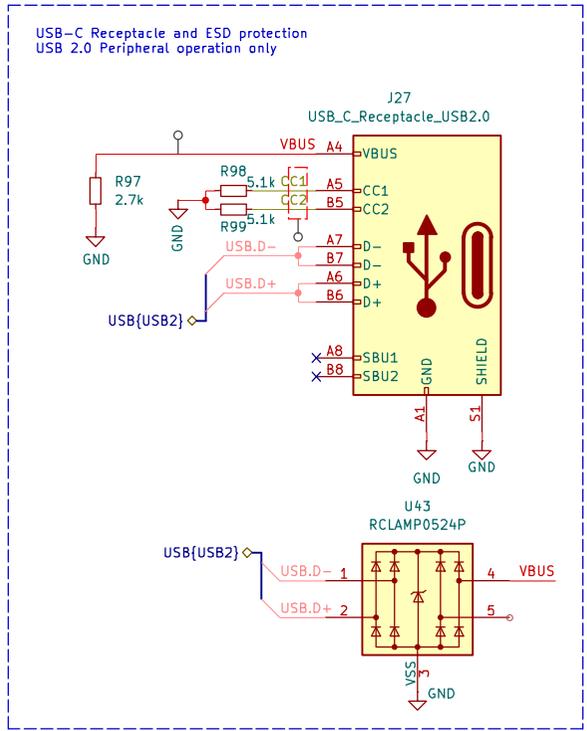
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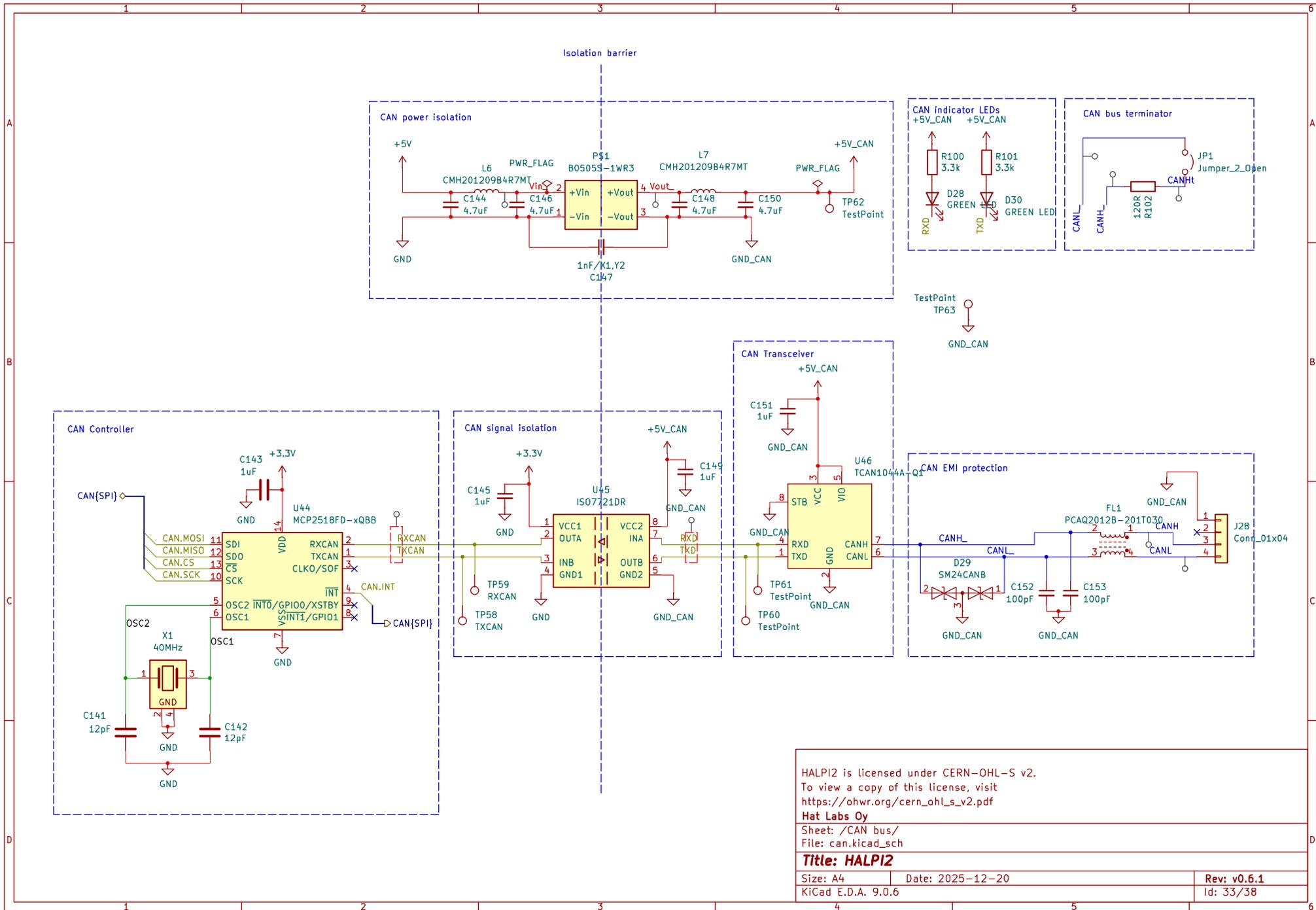
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Rev: v0.6.1
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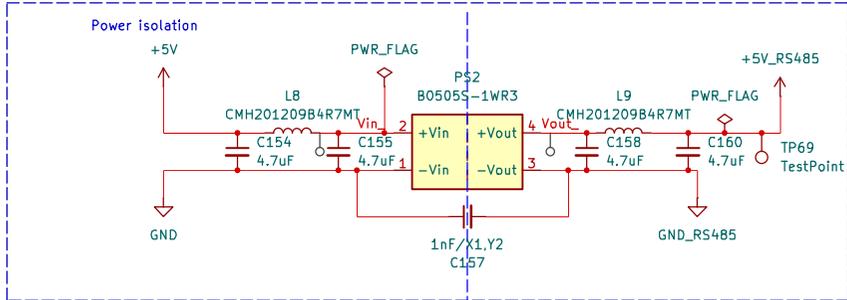


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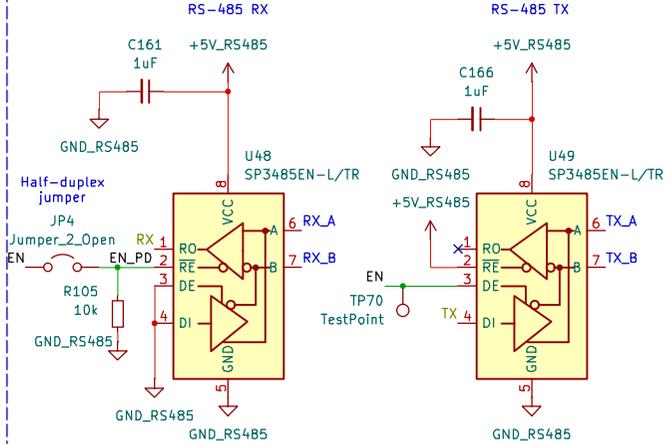
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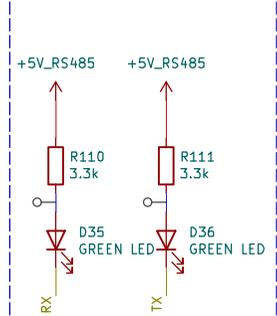
Isolation barrier



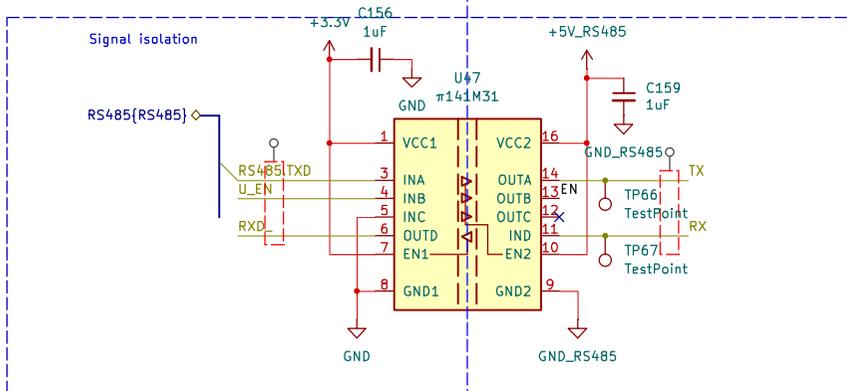
RS-485 Transceivers



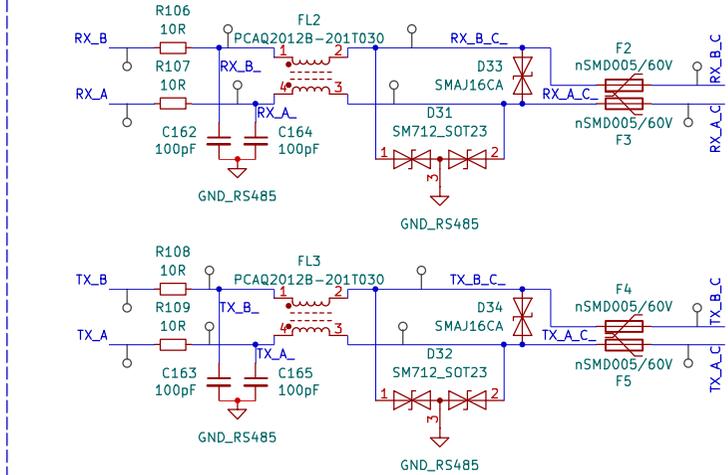
RS-485 Indicator LEDs



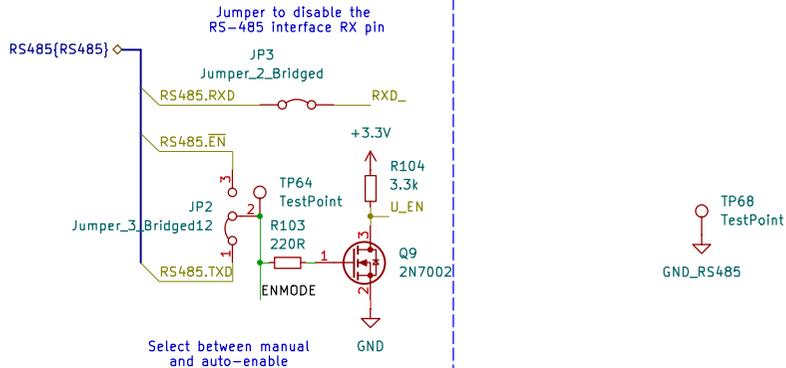
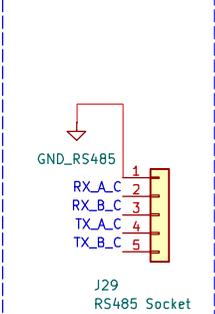
Signal isolation



RS-485 protection



Terminal Connector



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IMG1
HL logo



IMG5
Enclosure outline



IMG2
OSHW logo



IMG3
WEEE logo

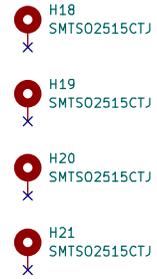


IMG4
CE logo

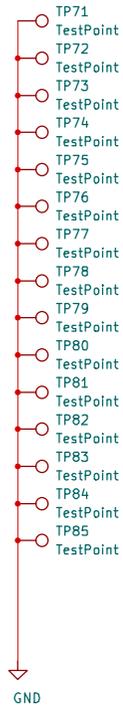
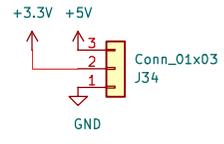
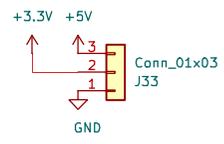
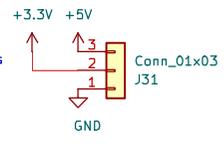
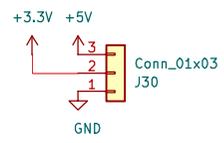
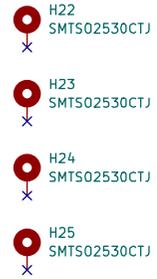
Mounting nut for PoE HAT



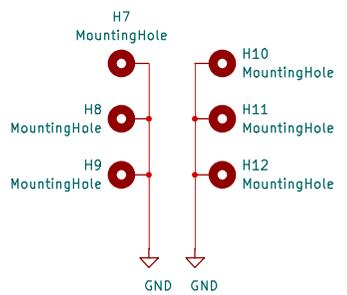
Mounting nuts for HAT corners



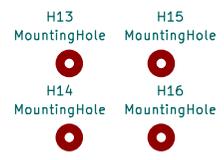
Mounting nuts for CMS corners



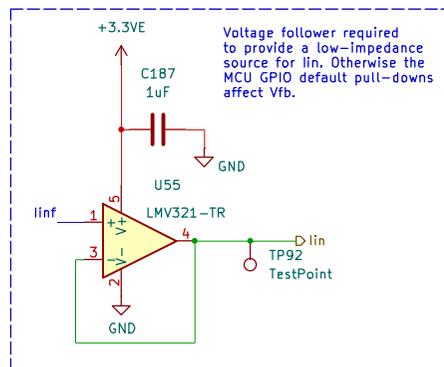
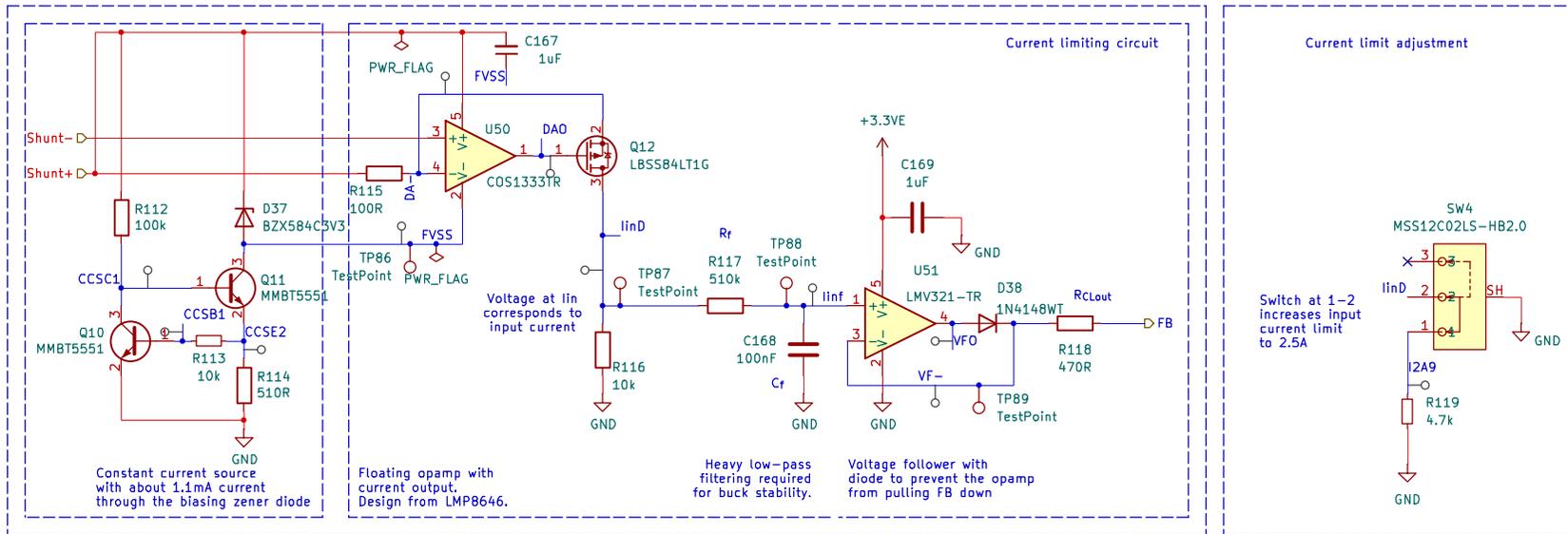
Board end mounting holes



Board corner mounting holes



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Size: A4	Date: 2025-12-20	Rev: v0.6.1
KiCad E.D.A. 9.0.6		Id: 35/38



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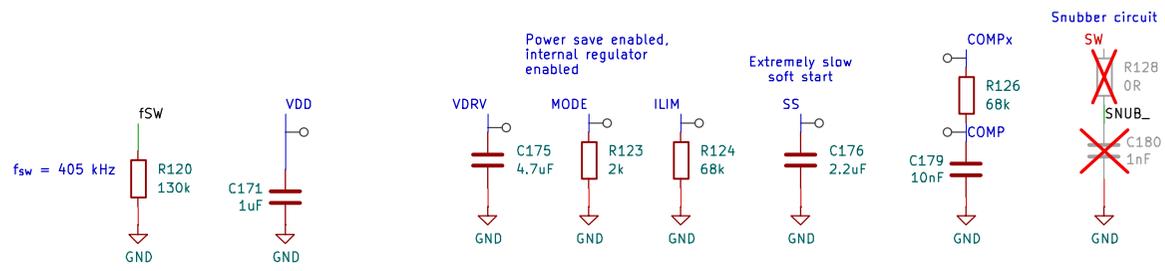
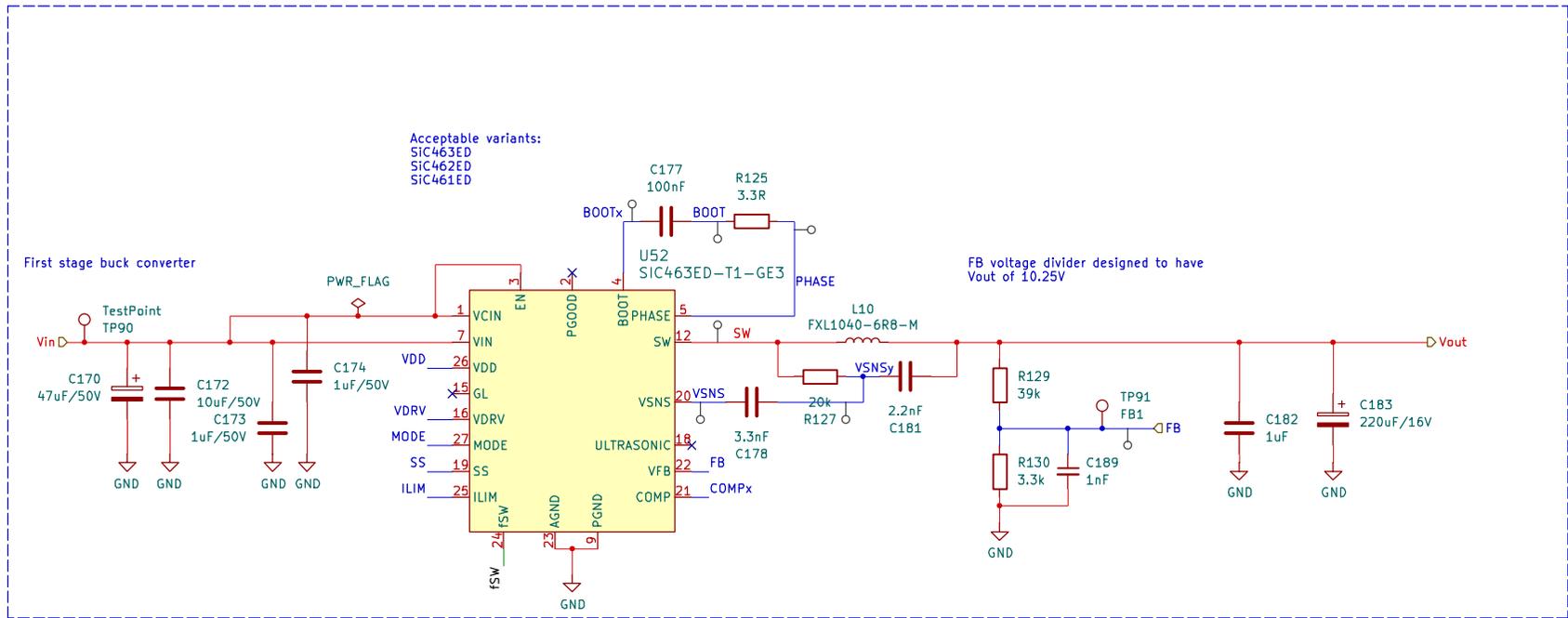
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Size: A4 Date: 2025-12-20

Rev: v0.6.1

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Id: 36/38

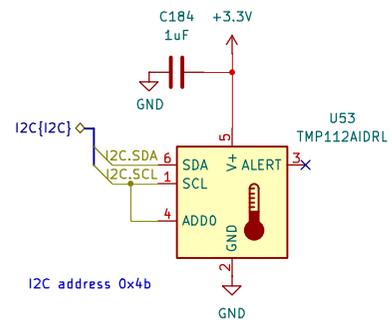


NOTE: If the converter is configured with a different SIC46x variant, ILIM must be adjusted as well (even for the same output current value).

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Size: A4	Date: 2025-12-20
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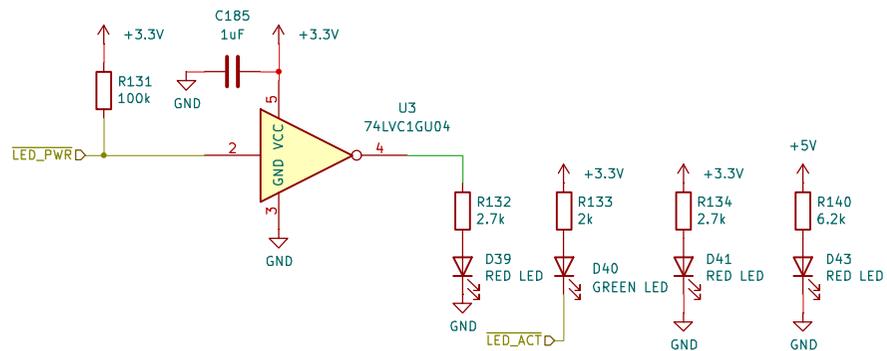
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Sheet: /Controller/MCU LEDs/
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